REMARKS

Claims 1-33 are all the claims pending in the application. Claims 1-33 stand rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. In addition, the specification stands objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The 35 U.S.C. §112, First Paragraph, Rejection

Claims 1-33 stand rejected under 35 U.S.C. §112, first paragraph. The Office Action argues that the claimed invention cannot observe data "within" a shift register if it removes the data, observes that data, and replaces the data; and that the phrase "without altering said data" cannot describe a situation where data is removed, observed, and replaced, without being destroyed. In response, the claims have been amended to define that the circuit and method are for "observing and restoring" the data "of" the shift register. Further, "altering" has been replaced with "altering logical values" to address these concerns.

While the foregoing claim changes have been made in order to address specific semantic preferences, Applicants note that the foregoing language modifications do not substantively change the breadth or meaning of the claims. Applicants respectfully submit that the statements in the Office Action regarding a restrictive meaning of what constitutes "altering" data within a shift register are unreasonable because the claims must be read in light the specification as they would be understood by one ordinarily skilled in the art. Applicants submit that a requirement that the phrase "without altering" mean that there can be no change, no matter how minor or insignificant, is an unreasonable requirement for the structure and method, especially as defined by the claims and described in the specification.

One ordinarily skilled in the art (especially after referencing the specification) would understand the phrase "without altering said data" to mean the process of removing data from the shift register, observing the data, and replacing the same data into the shift register without

altering the logical value of the data. The Office Action argues that there may be amplitude changes of the signal, or that the signal may be diminished as it progresses through the loop used for observation, and that the use changes do "alter" the data. This reasoning ignores the common meaning one ordinarily skilled in the art would apply to "alteration" in the claimed structure and method, because in this instance one ordinarily skilled in the art would understand that what is being altered (or not altered) is the logical value of the signal within the shift register. Thus, one ordinarily skilled in the art would understand that the previous phrase "without altering said data" meant that the logical value of the data is not logically changed by the processing and/or structure of the invention. Therefore, the addition of the foregoing claim language does not change the meaning of the claims from what they previously defined.

One ordinarily skilled in the art would understand the concern in this disclosure is to maintain the logical value of the data (e.g., logical zero or one). For example, paragraph 29 of the specification explains that the invention avoids using the standard LSSD scan clocks which destroy data in the rest of the latches on the chip, including latches within the circuit of interest, and restores data to the original position in latches. Therefore, one ordinarily skilled in the art would understand that if a logical zero or one were in a given position of a shift register before the processing of the claimed invention, that the same value would exist in the shift register after the processing of the invention. In that realm of understanding, the data is not "altered".

In the art field of the invention, it is of interest to be able to observe the state of latches for parts or all of the logic on the device without destroying the logical state of those latches. It is also an advantage for this observation not to require prior knowledge of the length of the shift register. The claimed invention provides a circuit and method for the circular shifting of varying length rotating shift registers and observation (or control) of each bit in the shift register during a circular shift process. The process ultimately restores the data back to the original positions in the latches of the shift register. In order to limit the need to have knowledge of any particular design, this invention also contains logic that can be used in a separate pre-operated mechanism to determine the length of each shift register that needs to be observed. This allows the method to work independently of any particular chip design.

Therefore, the specification as originally filed provides full and complete enablement for a structure and process that can observe data within shift registers without altering the logic of the data. The circuit includes selectors that selectively connect the input with the output of a selected shift register to form a wiring loop for the selected shift register. A control device connected to the wiring loop uses the wiring loop to cause the data to be continually transferred from the output of the selected shift register to the input of the selected shift register and back through the selected shift register in a circular manner. The control device includes a data output accessible from outside the circuit. An observation wire is connected to the wiring loop, and the data passes from the wiring loop to the control device through the observation wire. The control device outputs data appearing on the wiring loop as the data is circulated through the selected shift register to permit data within the selected shift register to be observed outside the circuit without altering the data within the selected shift register.

The inventive control device has a shift register selector connected to the selectors that cause the selectors to form the wiring loop using one or more different shift registers from the selected shift register. The control device can optionally include a storage device for recording the data as the data appears on the wiring loop. The invention can also include a write device for changing one or more bits of data within the shift register before the data is returned to the input of the shift register.

The invention uses the foregoing circuit to provide a method for observing data within a shift register without altering the data. The method selects a shift register from many shift registers and then continually transfers data from the output of the shift register to the input of the shift register and back through the shift register in a circular manner. The method outputs data as the data is transferred from the output of the shift register to the input of the shift register to permit data within the shift register to be observed outside the circuit without altering the data within the shift register. This allows the invention to send data to a location external to the shift register to allow the shift register to be examined by an external device.

Thus, the specification as originally filed provides full and complete support for the claimed invention and the Examiner is respectfully requested to reconsider and withdraw this

rejection.

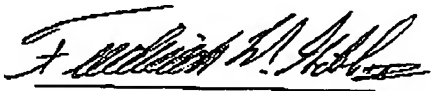
II. Formal Matters and Conclusion

With respect to the objection to the specification, the specification has been amended to change "multiplexor" to "demultiplexor" to overcome this objection. As explained in Applicants' previous response, such terms are used interchangeably by those ordinarily skilled in the art. Therefore, the addition of the term "demultiplexor" does not constitute "new matter" in that one ordinarily skilled in the art would understand that switches, multiplexors, demultiplexors, etc. were disclosed by the previous description and drawings. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the specification, claims and drawings.

In view of the foregoing, Applicants submit that claims 1-33, all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 6/21/05



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